Amendments to the Claims

1. (canceled)

2. (previously presented) A signal generator, comprising:
a synthesizer that generates a synthesizer signal which has a synthesizer frequency that corresponds to a tuning word and a clock signal;
a frequency controller that provides a controlled tuning word whose corresponding synthesizer frequency is within a selected frequency error from the reference frequency of a reference signal; and
a phase controller that alters the phase of said synthesizer signal to reduce a phase difference between said synthesizer signal and said reference signal;
wherein said frequency controller includes:
synthesizer and reference counters that respectively provide a synthesizer count of said synthesizer signal and a reference count of said reference frequency;
a differencer that obtains a difference count between said synthesizer count and said reference count; and
a count processor that processes said difference count into said controlled tuning word.

3. (previously presented) The generator of claim 2, wherein said count processor is configured to stop said counters when said reference count reaches a predetermined minimum count.

4. (previously presented) The generator of claim 2, wherein said frequency controller includes an adder that alters said controlled tuning word in response to a predetermined initial tuning word.

5. (previously presented) The generator of claim 2, wherein said frequency controller includes:
a frequency divider with a divisor S that couples said synthesizer signal to said synthesizer counter; and
a frequency multiplier that multiplies said controlled tuning word by a

multiplier S.

6. (currently amended) The generator of claim 2, wherein said phase controller includes:

a latch that provides a phase difference signal in response to said synthesizer signal and said reference signal; and

a digital filter that integrates said phase difference signal into a phase correction signal;

and the signal generator further including an adder that alters said synthesizer signal in response to said phase correction signal.

7. (original) The generator of claim 6, wherein said phase controller further includes an adder that offsets said phase difference signal in response to a selected phase offset signal.

8. (canceled)

9. (previously presented) The generator of claim 6, wherein said phase controller further includes:

a counter that provides a count between said synthesizer frequency and said reference frequency;

a multiplier that generates a correction factor in response to said count and a selected factor; and

another multiplier that alters said controlled tuning word with said correction factor.

10. (canceled)

11. (currently amended) The generator of claim 6, wherein said phase controller further includes:

another latch that receives said phase correction signal and is triggered by said reference signal to generate an output signal;

a differencer that provides a phase difference between said ~~first~~ phase correction signal and said output signal; and

a multiplier that alters said controlled tuning word with said phase difference.

12. (previously presented) The generator of claim 2, wherein said synthesizer is an accumulator.

13. (currently amended) ~~The~~ A signal generator ~~of claim 1~~, comprising:
a synthesizer that generates a synthesizer signal which has a synthesizer frequency that corresponds to a tuning word and a clock signal;
a frequency controller that provides a controlled tuning word whose corresponding synthesizer frequency is within a selected frequency error from the reference frequency of a reference signal; and
a phase controller that alters the phase of said synthesizer signal to reduce a phase difference between said synthesizer signal and said reference signal;
wherein said synthesizer is an accumulator that comprises:
an adder; and
a latch that receives an input signal from said adder and feeds an output signal back to said adder.

14. (currently amended) The generator of claim 13 ~~1~~, further including a word converter that alters at least one word of said synthesizer signal.

15. (original) The generator of claim 14, wherein said word converter includes a memory that stores at least one word of said synthesizer signal and a corresponding replacement word.

16. (currently amended) The generator stem of claim 13 ~~1~~, further including a digital-to-analog converter that converts said synthesizer signal to an analog synthesizer signal.

17. (previously presented) The generator of claim 2, further including a word converter inserted between said synthesizer and said digital-to-analog converter wherein said word converter alters at least one word of said synthesizer signal.

18. (previously presented) A signal generator, comprising:

a synthesizer that generates a synthesizer signal which has a synthesizer frequency that corresponds to a tuning word and a clock signal;

synthesizer and reference counters arranged to provide a synthesizer count of said synthesizer signal and a reference count of a reference signal that has a reference frequency;

a differencer that provides a difference count in response to said synthesizer count and said reference count;

a count processor configured to:

a) stop said difference count when said reference count reaches a predetermined minimum count; and

b) process said difference count into a controlled tuning word whose corresponding synthesizer frequency is within a selected frequency error from the reference frequency of a reference signal; and

a phase controller that alters the phase of said synthesizer signal to reduce a phase difference between said synthesizer signal and said reference signal.

19. (original) The generator of claim 18, further including an adder that alters said controlled tuning word in response to a predetermined initial tuning word.

20. (previously presented) The generator of claim 18, wherein said frequency controller further includes a frequency divider with a divisor S that couples said synthesizer signal to said synthesizer counter and a frequency multiplier that multiplies said controlled tuning word by a multiplier S.

21. (canceled)

22. (previously presented) A method of locking a synthesizer signal to a reference signal, comprising the steps of:

generating a synthesizer signal to have a synthesizer frequency that corresponds to a tuning word and a clock signal;

providing a controlled tuning word whose corresponding synthesizer frequency is within a selected frequency error from the reference frequency of said

reference signal; and

altering the phase of said synthesizer signal to reduce a phase difference between said synthesizer signal and said reference signal;

wherein said providing step includes the steps of:

obtaining a difference count between said synthesizer frequency and said reference frequency; and

processing said difference count into said controlled tuning word.

23. (original) The method of claim 22, wherein said obtaining step includes the step of continuing a reference count of said reference frequency until it at least equals a predetermined minimum count.

24. (previously presented) The method of claim 22, wherein said providing step includes the steps of modifying said controlled tuning word in accordance with at least one of a predetermined frequency multiple and a predetermined tuning word.

25. (previously presented) The method of claim 22, wherein said altering step includes the steps of:

sensing a phase difference signal in response to said synthesizer signal and said reference signal;

integrating said phase difference signal into a phase correction signal; and

altering said synthesizer signal in response to said phase correction signal.

26. (original) The method of claim 25, further including the step of offsetting said phase difference signal in response to a selected phase offset signal.

27. (original) The method of claim 25, further including the steps of:

sensing a detected frequency multiple between said synthesizer frequency and said reference frequency;

forming a difference between said detected frequency multiple and a predetermined frequency multiple; and

altering said controlled tuning word by said difference.

28. (original) The method of claim 25, further including the step of altering said controlled tuning word by a correction difference between a first phase correction signal and a later phase correction signal.

29. (original) The method of claim 28, further including the step of modifying said correction difference by a predetermined frequency multiple.

30. (currently amended) ~~The~~ A method of locking a synthesizer signal to a reference signal ~~claim 21~~, comprising the steps of:

generating a synthesizer signal to have a synthesizer frequency that corresponds to a tuning word and a clock signal;

providing a controlled tuning word whose corresponding synthesizer frequency is within a selected frequency error from the reference frequency of said reference signal; and

altering the phase of said synthesizer signal to reduce a phase difference between said synthesizer signal and said reference signal;

wherein said generating step includes the step of recursively adding said tuning word at a rate of said clock signal.

31. (previously presented) The method of claim 22, further including the step of substituting at least one stored word for a corresponding word of said synthesizer signal.

32. (currently amended) The method of claim 30 ~~21~~, further including the step of converting said synthesizer signal to an analog synthesizer signal.